WHAT IS CLAIMED IS:

1. A CDMA transmitter comprising:

a first baseband combiner capable of receiving N baseband chip streams, each of said N baseband chip streams comprising a sequence of chips, each chip having one of a positive amplitude value and a negative amplitude value, wherein said first baseband combiner combines chips from corresponding time slots in each of said N baseband chip streams to thereby generate a first composite baseband chip sequence;

a data processor coupled to said first baseband combiner capable of detecting a first peak amplitude in said first composite baseband chip sequence that exceeds a pre-determined maximum threshold and determining an amplitude and a polarity of a first compensation pulse associated with said first peak amplitude; and

a pulse generator coupled to said data processor capable of generating said first compensation pulse having said amplitude and said polarity determined by said data processor, wherein said first baseband combiner receives said first compensation pulse and combines said first compensation pulse with said first composite baseband chip sequence during a chip time slot corresponding to said first peak amplitude.

2. The CDMA transmitter as set forth in Claim 1 wherein said data processor determines said amplitude and said polarity of said first compensation pulse as a function of a maximum peak-to-average power ratio associated with said first composite baseband chip sequence.

3. The CDMA transmitter as set forth in Claim 2 wherein said each chip in each of said N baseband chip streams has one of a +1 relative amplitude value and -1 relative amplitude value.

4. The CDMA transmitter as set forth in Claim 3 wherein said CDMA transmitter is a quadrature phase-shift keying (QPSK) transmitter and said first composite baseband chip sequence is a composite in-phase chip sequence.

5. The CDMA transmitter as set forth in Claim 1 further comprising:

a second baseband combiner capable of receiving M baseband chip streams, each of said M baseband chip streams comprising a sequence of chips, each chip having one of a positive amplitude value and a negative amplitude value, wherein said second baseband combiner combines chips from corresponding time slots in each of said M baseband chip streams to thereby generate a second composite baseband chip sequence, wherein said data processor is coupled to said second baseband combiner and is further capable of detecting a second peak amplitude in said second composite baseband chip sequence that exceeds a pre-determined maximum threshold and determining an amplitude and a polarity of a second compensation pulse associated with said second peak amplitude; and

a second pulse generator coupled to said data processor capable of generating said second compensation pulse having said amplitude and said polarity determined by said data processor, wherein said second baseband combiner receives said second compensation pulse and combines said second compensation pulse with said second composite baseband chip sequence during a chip time slot corresponding to said second peak amplitude.

6. The CDMA transmitter as set forth in Claim 5 wherein said data processor determines said amplitude and said polarity of said second compensation pulse as a function of a maximum peak-to-average power ratio associated with said second composite baseband chip sequence.

7. The CDMA transmitter as set forth in Claim 6 wherein said each chip in each of said M baseband chip streams has one of a +1 relative amplitude value and -1 relative amplitude value.

8. The CDMA transmitter as set forth in Claim 7 wherein said CDMA transmitter is a quadrature phase-shift keying (QPSK) transmitter and said second composite baseband chip sequence is a composite quadrature chip sequence.

9. A wireless communication network comprising:

a plurality of base stations capable of communicating with a plurality of mobile stations disposed in a coverage are of said plurality of base stations; and

a CDMA transmitter associated with at least one of said plurality of base stations, said CDMA transmitter comprising:

a first baseband combiner capable of receiving N baseband chip streams, each of said N baseband chip streams comprising a sequence of chips, each chip having one of a positive amplitude value and a negative amplitude value, wherein said first baseband combiner combines chips from corresponding time slots in each of said N baseband chip streams to thereby generate a first composite baseband chip sequence;

a data processor coupled to said first baseband combiner capable of detecting a first peak amplitude in said first composite baseband chip sequence that exceeds a pre-determined maximum threshold and determining an amplitude and a polarity of a first compensation pulse associated with said first peak amplitude; and

a pulse generator coupled to said data processor capable of generating said first compensation pulse having

said amplitude and said polarity determined by said data processor, wherein said first baseband combiner receives said first compensation pulse and combines said first compensation pulse with said first composite baseband chip sequence during a chip time slot corresponding to said first peak amplitude.

10. The wireless communication network as set forth in Claim 9 wherein said data processor determines said amplitude and said polarity of said first compensation pulse as a function of a maximum peak-to-average power ratio associated with said first composite baseband chip sequence.

11. The wireless communication network as set forth in Claim 10 wherein said each chip in each of said N baseband chip streams has one of a +1 relative amplitude value and -1 relative amplitude value.

12. The wireless communication network as set forth in Claim 11 wherein said CDMA transmitter is a quadrature phase-shift keying (QPSK) transmitter and said first composite baseband chip sequence is a composite in-phase chip sequence.

13. The wireless communication network as set forth in Claim 7, wherein the CDMA transmitter further comprises:

a second baseband combiner capable of receiving M baseband chip streams, each of said M baseband chip streams comprising a sequence of chips, each chip having one of a positive amplitude value and a negative amplitude value, wherein said second baseband combiner combines chips from corresponding time slots in each of said M baseband chip streams to thereby generate a second composite baseband chip sequence, wherein said data processor is coupled to said second baseband combiner and is further capable of detecting a second peak amplitude in said second composite baseband chip sequence that exceeds a pre-determined maximum threshold and determining an amplitude and a polarity of a second compensation pulse associated with said second peak amplitude; and

a second pulse generator coupled to said data processor capable of generating said second compensation pulse having said amplitude and said polarity determined by said data processor, wherein said second baseband combiner receives said second compensation pulse and combines said second compensation pulse with said second composite baseband chip sequence during a chip time slot corresponding to said second peak amplitude.

14. The wireless communication network as set forth in Claim 13 wherein said data processor determines said amplitude and said polarity of said second compensation pulse as a function of a maximum peak-to-average power ratio associated with said second composite baseband chip sequence.

15. The wireless communication network as set forth in Claim 14 wherein said each chip in each of said M baseband chip streams has one of a +1 relative amplitude value and -1 relative amplitude value.

16. The wireless communication network as set forth in Claim 15 wherein said CDMA transmitter is a quadrature phase-shift keying (QPSK) transmitter and said second composite baseband chip sequence is a composite quadrature chip sequence.

17. A method of processing baseband chip streams in a CDMA transmitter, the method comprising the steps of:

receiving N baseband chip streams, each of the N baseband chip streams comprising a sequence of chips, each chip having one of a positive amplitude value and a negative amplitude value;

combining chips from corresponding time slots in each of the N baseband chip streams to thereby generate a first composite baseband chip sequence;

detecting a first peak amplitude in the first composite baseband chip sequence that exceeds a pre-determined maximum threshold;

determining an amplitude and a polarity of a first compensation pulse associated with the first peak amplitude;

generating the first compensation pulse having the determined amplitude and polarity; and

combining the first compensation pulse with the first composite baseband chip sequence during a chip time slot corresponding to the first peak amplitude.

18. The method as set forth in Claim 17 wherein the amplitude and the polarity of the first compensation pulse are determined as a function of a maximum peak-to-average power ratio associated with the first composite baseband chip sequence.

19. The method as set forth in Claim 18 wherein each chip in each of the N baseband chip streams has one of a +1 relative amplitude value and -1 relative amplitude value.

20. The method as set forth in Claim 17 further comprising the steps of:

receiving M baseband chip streams, each of the M baseband chip streams comprising a sequence of chips, each chip having one of a positive amplitude value and a negative amplitude value;

combining chips from corresponding time slots in each of the M baseband chip streams to thereby generate a second composite baseband chip sequence;

detecting a second peak amplitude in the second composite baseband chip sequence that exceeds a pre-determined maximum threshold;

determining an amplitude and a polarity of a second compensation pulse associated with the second peak amplitude;

generating the second compensation pulse having the determined amplitude and polarity; and

combining the second compensation pulse with the second composite baseband chip sequence during a chip time slot corresponding to the second peak amplitude.

21. The method as set forth in Claim 20 wherein the amplitude and the polarity of the second compensation pulse are determined as a function of a maximum peak-to-average power ratio associated with the second composite baseband chip sequence.

22. The method as set forth in Claim 21 wherein each chip in each of the M baseband chip streams has one of a +1 relative amplitude value and -1 relative amplitude value.